IN THE CLAIMS:

Please amend the claims as follows.

1. (Currently Amended) ~~An improved~~ A digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals that are different in frequency, phase or both frequency and phase; and

a feedback ~~means~~ circuit interconnecting said plurality of memory devices and cross-coupling signals produced by said plurality of memory devices.

2. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 1, further comprising:

a common frequency reference source in communication with said plurality of memory devices, said common frequency reference source ~~for~~ driving said plurality of memory devices.

3. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim ~~2~~ 1, wherein said multiple timing signals include at least one signal selected from the group consisting of an RF carrier signal, a data bit-rate signal, a data chip-rate signal, a data frame-rate signal, ~~and~~ a data burst-rate signal, ~~or~~ and a packet-rate signal.

4. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals are integrally or fractionally related in frequency, phase or both frequency and phase.

5. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said multiple timing signals are rationally ~~multiply~~ related in frequency and/or phase.

6. (Currently Amended) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals;

feedback means interconnecting said memory devices and cross-coupling signals produced by said memory devices; and

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices,

~~The improved digital-data receiver synchronization apparatus of claim 2,~~ wherein said multiple timing signals satisfy the relationship

$$f_1 = M \cdot f_2 = M \cdot N \cdot f_3$$

wherein f_1 is said RF signal; f_2 is said data bit rate signal; f_3 is said data frame-rate signal; and M and N are positive rational numbers.

7. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 2, wherein said common frequency reference source includes ~~is~~ an oscillator controlled by a crystal, SAW device, ceramic resonator, mechanical resonator, dielectric resonator, or external source.

8. (Currently Amended) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals;

feedback means interconnecting said memory devices and cross-coupling signals produced by said memory devices; and

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices.

~~The improved digital-data receiver synchronization apparatus of claim 2,~~ wherein said common frequency reference uses edge-triggered synchronous logic.

9. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim ~~2~~ 1, wherein ~~said~~ signals cross-coupled by said feedback ~~means~~ circuit include at least one ~~signal~~ member selected from the group consisting of error signals~~, output signals, and both error~~ and output signals.

10. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 1, wherein ~~said~~ signals cross-coupled by said feedback ~~means are~~ circuit include analog signals.

11. (Currently Amended) The ~~improved~~ digital-data receiver synchronization of claim 1, wherein ~~said~~ signals cross-coupled by said feedback ~~means are~~ circuit include digital signals.

12. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 1, wherein said plurality of memory devices ~~are~~ include phase-locked loops.

13. (Currently Amended) ~~An improved~~ A digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals that are different in frequency, phase or both frequency and phase, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback ~~means~~ circuit interconnecting said memory devices and for cross- coupling ~~certain~~ signals produced by said memory.

14. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 13, wherein said multiple timing signals include at least one of an RF signal, a data bit-rate signal, a data chip-rate signal, a data frame-rate signal, ~~and~~ a data burst signal, ~~or~~ and a data packet-rate signal.

15. (Currently Amended) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross- coupling certain signals produced by said memory devices,

~~The improved digital-data receiver synchronization apparatus of claim 13,~~ wherein said multiple timing signals satisfy the relationship:

$$f_1 = M \cdot f_2 = M \cdot N \cdot f_3$$

wherein f_1 is said RF signal; f_2 is said data bit-rate signal; f_3 is said data frame-rate signal; and M and N are positive rational numbers.

16. (Currently Amended) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross- coupling certain signals produced by said memory devices,

~~The improved digital-data receiver synchronization apparatus of claim 13,~~ wherein said common frequency reference uses edge-triggered synchronous logic.

17. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 13, wherein said signals cross-coupled by said feedback ~~means~~ circuit include at least one signal selected from the group consisting of error signals~~, output signals, and both error~~ and output signals.

18. (Currently Amended) The ~~improved~~ digital-data receiver synchronization apparatus of claim 13, wherein said composite phase-frequency detector comprises at least one device selected from the group consisting of: a digital phase detector; a digital phase-frequency detector; a standard analog RF mixer; a standard analog multiplier; a digital XOR gate; a digital J-K flip-flop; a digital trigger (T) flip-flop; a digital R-S flip-flop; and a digital counter~~;~~.

19. (Currently Amended) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross- coupling certain signals produced by said memory devices,

~~The improved digital-data receiver synchronization apparatus of claim 13,~~ wherein said composite phase-frequency detector further includes at least one device selected from the group consisting of a switch; a relay; a digital trigger (T) flip-flop; a digital divider; a nonlinear element; an analog divider; a square-root circuit; a comparator; a frequency-to-voltage converter; a frequency-to-current converter; a digital phase detector; a digital phase-frequency detector; a digital AND gate; a digital OR gate; a digital XOR gate; a digital counter; a digital J-K flip-flop; a digital R-S flip-flop; a majority-logic circuit; a peak detector; an average detector; a root-mean-square (RMS) detector; an operational amplifier; a follower circuit; a logic array device; a microprocessor; a digital state machine; a neural network; a digital signal processor (DSP) device; and an analog signal processor (ASP) device.

20. (Currently Amended) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross- coupling certain signals produced by said memory devices,

~~The improved digital-data receiver synchronization apparatus of claim 13,~~ wherein said composite phase-frequency detector comprises a timing device for limiting the detector signal pulse widths.

21. (Currently Amended) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross- coupling certain signals produced by said memory devices,

~~The improved digital-data receiver synchronization apparatus of claim 13,~~ wherein said composite phase-frequency detector further comprises at least one device selected from the group consisting of: a monostable multivibrator; a delay generator; a digital counter; a logic gate; a switch; a digital state machine; a pulse width-to-voltage converter; a pulse width-to-current converter; an integrator; a comparator; and a pulse width-limiting circuit.

22. (Currently Amended) An improved digital-data receiver synchronization apparatus comprising:

a plurality of memory devices for receiving multiple timing signals, at least one of said plurality of memory devices comprising a composite phase-frequency detector;

a common frequency reference source in communication with said plurality of memory devices for driving said plurality of memory devices; and,

a feedback means interconnecting said memory devices and for cross- coupling certain signals produced by said memory devices,

~~The improved digital-data receiver synchronization apparatus of claim 13,~~ wherein said composite phase-frequency detector further comprises an input-signal rate-limiting amplifier whereby said composite phase-frequency detector will not follow a signal having oscillations above a predetermined rate of change.

23. (Original) The improved digital-data receiver synchronization apparatus of claim 22, wherein said rate of change is measured in voltage (volts) per second.

24. (Original) The improved digital-data receiver synchronization apparatus of claim 22, wherein said rate of change is measured in current (amps) per second.

25. (Canceled)

26. (Canceled)

27. (Currently Amended) ~~The~~ A method of providing ~~improved~~ digital-data receiver synchronization comprising ~~the steps of~~:

providing a plurality of memory devices for receiving multiple timing signals that are different in frequency, phase or both frequency and phase, ~~at least one of said plurality of memory devices comprising a composite phase-frequency detector,~~ each of said plurality of memory devices providing an output comparison signal; and~~,~~

interconnecting said plurality of memory devices with a feedback ~~means~~ circuit ~~for~~ that cross-couples ~~cross-coupling~~ said output comparison signals produced by each of said plurality of memory devices. that are different in frequency, phase or both frequency and phase.

28. (Currently Amended) The method according to claim 27, further comprising ~~the step of~~:

connecting a common frequency reference source to ~~with~~ said plurality of memory devices, said common frequency reference source ~~for~~ driving said plurality of memory devices.

29. (Canceled)

30. (New) The method according to claim 27, wherein at least one of said plurality of memory devices includes a composite phase-frequency detector.